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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Kiyotaka Imai

Serial No.: 09/828,862

Group Art Unit: 2811

Filed: April 10, 2001

Examiner: Quang Vu

For: SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME

Honorable Commissioner of Patents
Washington, D.C. 20231

AMENDMENT UNDER 37 C.F.R. § 1.111

Sir:

In response to the Office Action dated December 19, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims to read as follows:

3. (Amended) A method for manufacturing a semiconductor device comprising:

implanting arsenic ions in a semiconductor substrate at a first acceleration energy level which suppresses a reverse channel effect to form arsenic ion implanted regions;

implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting, at a second acceleration energy level lower than the first acceleration energy level, so as to form a concentration peak of the phosphorous ions located in the arsenic ion implanted regions, a phosphorous ion-implanted region extending beyond said arsenic ion-implanted region; and

heat-treating the ion-implanted regions for activation of the arsenic ions and the phosphorous ions to form source/drain regions.

4. (Amended) The method as defined in claim 3, wherein n-type impurities are implanted in said substrate to form an n-type extension region before the arsenic and phosphorous implanting.